EPITAXIAL GROWTH METHOD

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BACKGROUND

[0001] Fig. 1 illustrates a conventional MOSFET 10. The device is formed in a p-well or an n-well 11 formed in a silicon substrate (not shown). A channel 12 is then doped by, for example, ion implantation. A high dielectric constant (k) film 15 is then formed over the device by chemical vapor deposition (CVD) or sputtering. The gate, typically poly silicon or metal, is then formed over the high k film. Portions of the gate and the high k film are then etched away to expose source/drain regions 13, which are then doped.

[0002] The device is annealed, typically at about 1100°C, to activate the p- and n-type dopants. During the high temperature anneal, the channel region 12 and the high k layer 15 react to form an interfacial layer 14. The interfacial layer and the high k film together have a lower capacitance than the high k film alone. The reduced capacitance caused by interfacial layer 14 reduces the driving current of the device and thereby reduces the operating speed of the device.

SUMMARY

[0003] In accordance with a first embodiment of the invention, a MOSFET includes a well, a channel formed in the well, a high K layer overlying the channel, a buffer layer overlying the high k layer, a gate overlying the buffer layer, a blocking layer overlying the gate and two source/drain regions. In some embodiments the high k layer is an epitaxial metal oxide. In embodiments the buffer and blocking layers are epitaxial silicon. In some embodiments the gate and the source/drain regions are amorphous silicon germanium. In accordance with another embodiment of the invention, a MOSFET includes a well, a channel formed in the well, a high K layer overlying the channel, a metal gate overlying the high k layer, and two silicon germanium source/drain regions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1 illustrates a prior art MOSFET.

[0005] FIGS. 2-8 illustrate an embodiment of the present invention at various stages in fabrication.

[0006] FIG. 9 illustrates an epitaxial high k layer.

[0007] FIG. 10 illustrates another embodiment of the present invention.

DETAILED DESCRIPTION

[0008] In accordance with embodiments of the invention, the source/drain regions and/or the gate of a MOSFET are silicon/germanium.

[0009] FIGS. 2-8 illustrate the fabrication of one embodiment of the present invention. Referring now to FIG. 2, first an n-well or a p-well 20 is formed on a substrate (not shown). The channel 25 of the device is implanted with a p- or n-type dopant, depending if the device is a p-channel device or an n-channel device. A common p-type dopant is boron, and common n-type dopants are phosphorus or arsenic.

[0010] In FIG. 3, a high k layer 21 is grown over the substrate including the implanted channel. High k layer may be, for example, a metal oxide, such as, for example, zircon oxide, titanium oxide, tantalum oxide, or hafnium oxide. The high k layer is grown epitaxially as illustrated in FIG. 9. The high k layer includes alternating monolayers of oxygen 21a and metal 21b. Epitaxial high k layer 21, and other epitaxial layers described below, may be grown, for example, by molecular beam epitaxy (MBE), chemical vapor deposition (CVD) or other epitaxial techniques. The high k layer is thick enough to have a leakage current blocking capability equivalent to ten angstrom thick layer of SiO_2. The appropriate thickness of the high k layer can be determined as follows. The thickness of the high k layer is defined by the boundary equation $e_1E_1 = e_2E_2$, where e is a dielectric constant and E is the electric field, given by the applied bias in volts divided by the material thickness. The boundary equation therefore simplifies to $e_1/t_1 = e_2/t_2$, where t is the material thickness. For a given high k material, the required thickness can be determined by plugging in the dielectric constant of SiO_2 and a ten angstrom thickness of SiO_2 on the left hand side of the equation, plugging in the dielectric constant of the selected high k material, then solving for t_2.

[0011] After the epitaxial high k layer is grown, an epitaxial silicon buffer layer 22 is grown over the high k layer. Usually, the bufer layer is less than ten layers of atomic undoped silicon, preferably 2 to 3 layers.

[0012] Gate 23 is then deposited over buffer layer 22, as illustrated in FIG. 4. Gate 23 may be, for example, an epitaxial layer containing silicon and germanium. A blocking layer 24, similar to buffer layer 22, is deposited over gate 23. Blocking layer 24 may be, for example, an epitaxial silicon layer. Usually, the blocking layer is less than ten layers of atomic undoped silicon, preferably 2 to 3 layers. The presence of buffer layer 22 prevents germanium from gate 23 from contaminating high k layer 21 during thermal cycling. Similarly, the presence of blocking layer 24 prevents germanium from gate 23 from vaporizing during thermal cycling. In some embodiments, buffer layer 22 and blocking layer 24 are thin layers, on the order of only a few layers of silicon atoms thick.

[0013] Turning now to FIG. 6, portions of high k layer 21, buffer layer 22, gate 23, and blocking layer 24 are etched away, for example in an anisotropic etch, to expose the areas of well 20 where the source/drain regions will be formed. In a second etch, for example, an isotropic etch, illustrated in FIG. 7, portions of well 20 are removed. In one embodiment, a single etch removes portions of high k layer 21, buffer layer 22, gate 23, blocking layer 24, and well 20. Depending on the size of the device, the source/drain regions may be about 100 to 1000 angstroms deep.

[0014] In FIG. 8, the source/drain regions 25 of the device are formed in the spaces left by the removal of portions of well 20. Source/drain regions 25 may be, for example, amorphous or epitaxial silicon and germanium. New material is grown in the spaces in well 20 to form source/drain regions 25. Source/drain regions 25 are then doped. A contact, for example titanium nitride or nickel nitride (not shown) is then deposited over blocking layer 24.

[0015] FIG. 10 illustrates a second embodiment of the invention. A metal gate 39 is used instead of a silicon germanium gate. Thus, the buffer layer and blocking layer described above are not necessary to prevent migration of germanium.

[0016] In accordance with embodiments of the invention, a device with a silicon/germanium source/drain region and/or a silicon/germanium gate may offer advantages.

[0017] First, the presence of germanium in the gate and/or the source/drain regions of the device may lower the temperature at which the device is annealed to activate dopants in the channel region. Typically, as described above, devices such as that illustrated in FIG.1 are

annealed at temperatures of about 1050°C to 1100°C to activate dopants in the channel. Annealing at temperatures of 1050°C or 1100°C can destroy the channel by diffusion between the source/drain regions. In devices such as that illustrated in FIG. 8, annealing temperatures as low as 750°C, usually 850°C to 900°C, have been observed to be effective at activating the dopants. Lower processing temperature reduces or eliminates the interfacial layer shown in the device illustrated in FIG. 1 and reduces the amount of diffusion between the source/drain regions. Elimination of the interfacial layer may increase the capacitance of the device, which increases the speed of the device.

[0018] Second, elimination of interfacial layer 14 of FIG. 1 increases the operating speed of the device by increasing the capacitance. In addition, elimination of the interfacial layer reduces the problem of leakage current in the channel. High k layer 21 is a more effective leakage current blocker than interfacial layer 14 of FIG. 1. As a result, for the same leakage current blocking effectiveness, a high k layer 21 can be thinner than the high k layer/interfacial layer combination of FIG. 1. A thinner layer has higher capacitance and therefore faster operating speed than a thicker layer. Accordingly, for the same operating speed, a device without interfacial layer 14 may block more leakage current than a device with interfacial layer 14.

[0019] Third, the presence of germanium in gate 23 may make the gate more conductive.

[0020] While particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that changes and modifications may be made without departing from the invention in its broader aspects and, therefore, the appended claims are to encompass within their scope all such changes and modifications as fall within the true spirit and scope of this invention.